



# Two New and Novel Cascaded Multilevel Inverters with Less Number of Components Utilizing Series Submultilevel Inverters

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## Abstract

In this paper, two new cascaded inverters are proposed, by using the series connection of new Submultilevel inverters. Each of the proposed Submultilevel inverters consists of three batteries and eight power switches. Four algorithms are presented to determine the voltages of these batteries for each of the proposed structures. In this study the comparison between the proposed structures with conventional structures has been done. At first, the proposed algorithms of new structures are compared with each other and after that comparisons between proposed structures based on selected algorithms and the traditional structures are performed. This comparison shows that the proposed inverters can produce high number of output voltage levels due to determined number of power electronic switches. Also blocked voltage of the proposed structures is smaller than other compared structures which leads to reduce size and weight of the proposed inverters. Other advantages of these structures are reduction of voltage sources number, DC sources variety, the conduction losses and the number of power diodes. In order to demonstrate the correct operation of the proposed structures and applied algorithms, simulation results by using PSCAD/EMTDC software are shown.

*Keywords:* Cascaded inverter; DC/AC converter; Blocked voltage; Conduction loss; Submultilevel inverter.

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## 1. Introduction

Multilevel inverters are power electronic converters which produce a sinusoidal waveform with a combination of power electronic devices and DC voltage sources with low amplitude [1]. In recent years application of this type of converters has increased which could be effected by increasing use of DC voltage sources, such as fuel cells and solar cells on the one hand and increasing the number of hybrid vehicles on the other hand [2]. Some of advantages of multilevel inverter are high power quality, low electromagnetic interference, low losses and high voltage capability [3], but there are some disadvantages in this kind of converter. For example, the high number of power electronic switches, isolated DC voltage sources and the complexity of the control circuits and modulation methods are some disadvantages of this type of inverter [4-5]. Generally multilevel inverters are divided to three categories [24], diode clamped, floating capacitors, and cascade inverters which cascade inverter

performance are better than other type of inverters because of their high quality of output waveform due to high voltage levels, being modular and easy debugging. But one of the most disadvantages of these inverters is their high number of voltage sources [6-7]. The number of power electronic components such as switches, diodes, DC voltage sources, the total blocking voltage of switches and output voltage waveform quality are important in multilevel inverters. So in order to do a comparison between the different multilevel inverters, so-called parameters are used [8-9]. Nowadays several structures are suggested as cascade multilevel inverters that their purpose is to improve the mentioned parameters. Also some algorithms to determine the DC voltage sources in all these structures used to make these parameters better. It is clear that without appropriate algorithms to calculate the input sources amplitude, it is impossible to improve inverter parameters [10-12]. In fact, the

main purpose of new articles is reducing of number of components in multilevel inverters that is done in three ways: using of asymmetric sources instead of identical DC sources [13-15]; topological modification [16-19] and combination of both of them [20-21].

In this paper, two new proposed cascade structures are presented by cascading basic blocks (Submultilevel inverters) and it should be noted that each of these blocks can be used alone as an inverter. Size of DC voltage sources in the proposed inverters are calculated based on four different algorithms, and equations of the inverter parameters for each algorithm are calculated and compared separately. In the following, four algorithms which have better features, are selected among eight algorithms for comparison with the conventional inverters, and a comparison in case of the number of switches, IGBTs, diodes, drivers and total blocked voltage of switches, and also normalized blocked voltage, number of input voltage sources, variety of them and number of components in current-flow path has been done. Finally to demonstrate the validity of the proposed structures and algorithms, simulation results are shown.

## 1. The Proposed Inverters And Operation Performance

### A) Proposed submultilevel structures

In Fig. 1 the proposed Submultilevel inverters with three DC voltage sources are shown. As can be seen, these structures are made by three DC voltage sources and eight unidirectional power electronic switches. Switches in these structures can be used in 16 different states which are shown in Table I. In these structures, switches of  $S_1$ ,  $S_2$ ,  $T_1$  and  $T_2$  should not be turned on with switches  $S'_1$ ,  $S'_2$ ,  $T'_1$  and  $T'_2$  simultaneously, otherwise it will cause a short circuit of DC voltage sources. For example, when the switch  $S_1$  is turned on switch  $S'_1$  should not be turned on. It should be noted that there are a similar number of devices in the first and second proposed structures which show in Fig. 1(a) and Fig. 1(b) respectively except that how to connect devices such as voltage sources and power electronic switches.

The output voltages of first and second proposed structures for different switching states are shown in Table I. As this table shows, each of output voltage levels is produced by four turned on switches {R1-3} and with respect to the algorithms, in order to determine the DC voltage sources which discuss in next part, these structures can produce all even and odd voltage levels to have a sinusoidal output waveform. In the multilevel inverters the number of

output voltage levels are directly depends on the size of the DC voltage sources [22]

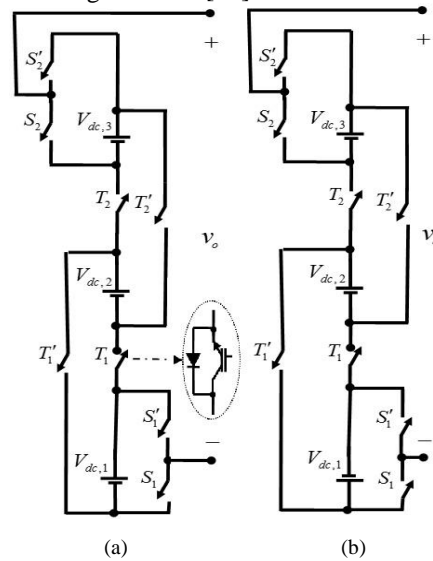


Fig. 1. a) first and b) second proposed Submultilevel inverters

which are determined by the proposed algorithms. For instance in order to create the level of  $V_{dc,1} + V_{dc,3}$  in state of 6 and according to second proposed structure, switches  $S'_1$ ,  $T'_1$ ,  $T_2$  and  $S'_2$  should be ON. In general, to determine the size of input sources the algorithms are divided into two categories: symmetric and asymmetric which each of them has specific applications. For example, a symmetric algorithm is very suitable for implementation of a various modulation methods, whereas asymmetric algorithms usually are used to produce more output voltage levels in the base frequency. Another comparison criterion of multilevel inverter is maximum blocked voltage by switches. To determine type and nominal ranges of IGBTs, the maximum blocked voltage (switch voltage stress) and the passing current of them is important. The value of maximum blocked voltage for each switch is shown in Table (2).

### B) Cascaded proposed inverters

In order to achieve higher output levels, several proposed Submultilevel inverters as shown in Fig. 1, can be connected in series, as shown in Fig. 2. In this structure, the first, second,  $\dots$  and  $n^{\text{th}}$  units, have DC voltage sources with sizes  $(V_{dc,1}, V_{dc,2}, V_{dc,3})$ ,  $(V_{dc,4}, V_{dc,5}, V_{dc,6})$ ,  $\dots$  and  $(V_{dc,3n-2}, V_{dc,3n-1}, V_{dc,3n})$  respectively where  $n$  is the number of series units. Based on Fig. 2, the output voltage of the proposed inverter is achieved by sum of Submultilevel inverters output voltage according to (1).

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \dots + v_{o,n}(t) \quad (1)$$

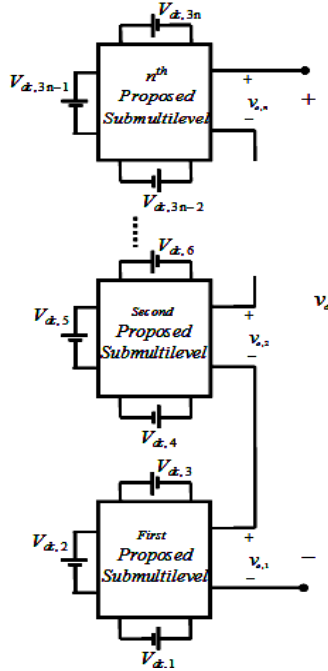


Fig. 2. Cascade proposed structure

According to the structures which used for unidirectional power electronic switches, the number of switches ( $N_{switch}$ ), IGBTs ( $N_{IGBT}$ ), diodes ( $N_{diode}$ ) and driver circuits ( $N_{driver}$ ) in proposed cascade structures, are same in this paper. It is important that the antiparallel diodes in the basic proposed structure are considered to pass reverse current which caused by inductive loads and in the absence of them this structure is only suitable for the resistive load. The values of these parameters and number of DC voltage sources ( $N_{source}$ ) are calculated in the following.

$$N_{switch} = N_{IGBT} = N_{diode} = N_{driver} = 8n \quad (2)$$

$$N_{source} = 3n \quad (3)$$

## 2. Algorithms To Determine The Value of DC Voltage Sources

In this section, all of the algorithms are in asymmetric mode. The main purpose of these algorithms is improving the quality of the output voltage waveform by increasing the number of voltage levels. As before mentioned, cascade inverter has a large number of isolated DC links that there are several ways to provide them. For example, using a transformer with isolated outputs which its outputs are used as the input voltage source after rectification and regulation or using combination of solar cells or fuel cells, or using DC/DC converters. For simplicity

in this paper, adjustable voltage sources are used as isolated DC voltage links. There are several methods to determine size of the input sources that all of them have a same power circuit. In following possible algorithms to determine the size of DC voltage sources in the first and second cascade proposed structures are investigated and required equations are calculated.

### A) DC voltage sources determination algorithms of second cascade proposed inverter

#### 1 First algorithm ( $A_1$ )

DC voltage sources in the first algorithm are identical in each basic block,  $\{R1-1\}$  then 7 is the number of voltage levels for each blocks while each block voltage sources are different from other blocks voltage sources. In the following, the value of input DC voltage sources in this algorithm, the number of output voltage levels ( $N_{level}$ ), variety of DC voltage sources ( $N_{variety}$ ), the maximum output voltage ( $V_{o,max}$ ), blocked voltage of  $n^{th}$  switch ( $V_{block,Sn}$ ), the total blocked voltage ( $V_{block}$ ) and normalized blocked voltage ( $V_{block,Norm}$ ) of the first cascade proposed structure are calculated and curves of these parameters will be shown in comparison study part. It should be noted that the normalized blocked voltage is not depends on algorithms, therefore in other algorithms computation, this parameter is ignored. In addition the output voltage of the first proposed inverter blocks in all possible states is shown in Table III.

$$V_{dc,(3j)} = V_{dc,(3j-1)} = V_{dc,(3j-2)} = 7^{j-1}V_{dc} \quad j = 1, 2, \dots, n \quad (4)$$

$$N_{level} = 7^n \quad (5)$$

$$N_{variety} = n \quad (6)$$

$$V_{o,max} = \frac{7^n - 1}{2} V_{dc} \quad (7)$$

$$V_{block,Sn} = \begin{cases} 7^{n-1}V_{dc} & S_{1,n}, S'_{1,n}, S_{2,n}, S'_{2,n} \\ 2(7^{n-1})V_{dc} & T_{1,n}, T'_{1,n}, T_{2,n}, T'_{2,n} \end{cases} \quad (8)$$

$$V_{block} = 2(7^n - 1)V_{dc} \quad (9)$$

$$V_{block,Norm} = \frac{V_{block}}{V_{o,max}} = 4 \quad (10)$$

#### 2 Second algorithm ( $A_2$ )

In the second algorithm, value of DC voltage sources is different in each basic block, while each of the series blocks are the same. In this algorithm the

output voltage levels are reduced in comparison with  $A_1$  but since each basic block structure is identical, the circuit complexity is reduced and because of extra switching states, it is very suitable for high frequency modulation applications. In the following the related equations are obtained for first cascade structure according to  $A_2$ . Also, output voltage of each blocks are shown in Table IV.

$$3V_{dc,3j} = 2V_{dc,(3j-1)} = 6V_{dc,(3j-2)} = 6V_{dc} \quad j=1,2,\dots,n \quad (11)$$

$$N_{level} = 12n + 1 \quad (12)$$

$$N_{variety} = 3 \quad (13)$$

$$V_{o,max} = 6nV_{dc} \quad (14)$$

$$V_{block,Sn} = \begin{cases} V_{dc} & S_{1,n}, S'_{1,n} \\ 2V_{dc} & S_{2,n}, S'_{2,n} \\ 4V_{dc} & T_{1,n}, T'_{1,n} \\ 5V_{dc} & T_{2,n}, T'_{2,n} \end{cases} \quad (15)$$

$$V_{block} = 24nV_{dc} \quad (16)$$

### 3 Third algorithm ( $A_3$ )

Output voltage levels of third and second algorithms are the same but variety of DC voltage sources is reduced in  $A_3$ . In fact, this algorithm has the minimum variation of input voltage sources among presented algorithms in this section. The number of output voltage levels, the maximum output voltage amplitude and total blocked voltage in this algorithm is similar to the ( $A_2$ ) algorithm and other equations are obtained in following and Submultilevel inverters output voltage are shown in table IV.

### 4 Fourth algorithm ( $A_4$ )

In comparison with algorithms which proposed so far, the fourth algorithm, can produce the maximum number of output voltage levels with less variety of DC voltage sources. The main purpose of this algorithm is to improve the quality of the output voltage waveform due to certain number of power switches. The value of DC voltage sources in the first cascade proposed structure is matched with (20). {R1-1} In this equation the 13 is referred to the maximum number of output voltage levels for each Submultilevel inverters. In following the related equations are obtained for first cascade structure

according to  $A_4$ . Also, output voltage of each block is shown in Table V.

$$V_{dc,3j} = 4V_{dc,(3j-1)} = 4V_{dc,(3j-2)} = 4V_{dc} \quad j=1,2,\dots,n \quad (17)$$

$$N_{variety} = 2 \quad (18)$$

$$V_{block,Sn} = \begin{cases} V_{dc} & S_{1,n}, S'_{1,n} \\ 4V_{dc} & S_{2,n}, S'_{2,n} \\ 2V_{dc} & T_{1,n}, T'_{1,n} \\ 5V_{dc} & T_{2,n}, T'_{2,n} \end{cases} \quad (19)$$

$$V_{dc,3j} = 4V_{dc,(3j-1)} = 4V_{dc,(3j-2)} = 4(13^{j-1})V_{dc} \quad j=1,2,\dots,n \quad (20)$$

$$N_{level} = 13^n \quad (21)$$

$$N_{variety} = 2n \quad (22)$$

$$V_{o,max} = \sum_{j=1}^n V_{dc,j} = V_{dc} + V_{dc} + 4V_{dc} + 13V_{dc} + 13V_{dc} + 52V_{dc} + \dots + 13^{n-1}V_{dc} + 13^{n-1}V_{dc} + 4(13^{n-1})V_{dc} = \left(\frac{13^n - 1}{2}\right)V_{dc} \quad (23)$$

$$V_{block,Sn} = \begin{cases} 13^{n-1}V_{dc} & S_{1,n}, S'_{1,n} \\ 4(13^{n-1})V_{dc} & S_{2,n}, S'_{2,n} \\ 5(13^{n-1})V_{dc} & T_{1,n}, T'_{1,n} \end{cases} \quad (24)$$

$$V_{block} = 2 \sum_{j=1}^n (V_{block,S1,j} + V_{block,S2,j} + V_{block,T1,j} + V_{block,T2,j}) = 2(13^n - 1)V_{dc} \quad (25)$$

## B) DC voltage sources determination algorithms of second cascade proposed inverter

### 1 First algorithm ( $B_1$ )

The first algorithm to determine the value of DC voltage sources in second cascade proposed inverter is the binary algorithm, which known as a geometric progression with ratio 2. In this algorithm, all Submultilevel inverters are the same, so it is very simple and suitable to implement for applications in high frequency modulation. The number of output voltage levels, variety of them, the maximum output voltage amplitude and total blocked voltage in this algorithm is similar to the  $A_2$ . So normalized blocked voltage in this structure and first structure are the same and it is equal to 4. The value of input

DC voltage sources and blocked voltage of  $n^{\text{th}}$  switch are presented as following equations and all the possible states of Submultilevel inverters output voltage are shown in Table IV.

$$2V_{dc,3j} = V_{dc,(3j-1)} = 4V_{dc,(3j-2)} = 4V_{dc} \quad j=1,2,\dots, \quad (26)$$

$$V_{block,Sn} = \begin{cases} V_{dc} & S_{1,n}, S'_{1,n} \\ 2V_{dc} & S_{2,n}, S'_{2,n} \\ 3V_{dc} & T_{1,n}, T'_{1,n} \\ 6V_{dc} & T_{2,n}, T'_{2,n} \end{cases} \quad (27)$$

## 2 Second algorithm (B<sub>2</sub>)

In this algorithm, the value of DC voltage sources in first block is similar to the previous algorithm but value of them in others is selected to increase the number of output voltage levels. In following the related equations are obtained according to B<sub>2</sub>. Also, output voltages of each Submultilevel inverter are shown in Table V. {R1-1} In (29), 13 is referred to the number of output voltage levels for each Submultilevel inverters in the binary algorithms.

$$2V_{dc,3j} = V_{dc,(3j-1)} = 4V_{dc,(3j-2)} = 4(13^{j-1})V_{dc} \quad j=1,2,\dots, \quad (28)$$

$$N_{level} = 13^n \quad (29)$$

$$N_{variety} = 3n \quad (30)$$

$$V_{o,max} = \sum_{j=1}^n V_{dc,j} \quad (31)$$

$$= 4V_{dc} + 2V_{dc} + 52V_{dc} + 26V_{dc} + \dots + 4(13^{n-1})V_{dc} + 2(13^{n-1})V_{dc}$$

$$= \left(\frac{13^n - 1}{2}\right)V_{dc}$$

$$V_{block,Sn} = \begin{cases} 13^{n-1}V_{dc} & S_{1,n}, S'_{1,n} \\ 2(13^{n-1})V_{dc} & S_{2,n}, S'_{2,n} \\ 3(13^{n-1})V_{dc} & T_{1,n}, T'_{1,n} \\ 6(13^{n-1})V_{dc} & T_{2,n}, T'_{2,n} \end{cases} \quad (32)$$

## 3 Third algorithm (B<sub>3</sub>)

Output voltage levels of B<sub>2</sub>, B<sub>3</sub> are the same, but variety of DC voltage sources in B<sub>3</sub> is less than B<sub>2</sub>. Main purpose of this algorithm is reduction of variety of DC voltage sources. The value of DC voltage sources which used in this algorithm is based on the (33). The number of output voltage levels, the maximum output voltage amplitude and total blocked

voltage in this algorithm is similar to B<sub>2</sub>. The value of the input DC voltage sources, variety of them and blocked voltage of  $n^{\text{th}}$  switch are achieved as following equations. Also output voltages of Submultilevel inverters are shown in table V.

$$V_{dc,3j} = V_{dc,(3j-1)} = 3V_{dc,(3j-2)} = 3(13^{j-1})V_{dc} \quad j=1,2,\dots, \quad (33)$$

$$N_{variety} = 2n \quad (34)$$

$$V_{block,Sn} = \begin{cases} 13^{n-1}V_{dc} & S_{1,n}, S'_{1,n} \\ 3(13^{n-1})V_{dc} & S_{2,n}, S'_{2,n} \\ 2(13^{n-1})V_{dc} & T_{1,n}, T'_{1,n} \\ 6(13^{n-1})V_{dc} & T_{2,n}, T'_{2,n} \end{cases} \quad (35)$$

## 4 Fourth algorithm (B<sub>4</sub>)

The last proposed algorithm of the second cascade proposed structure is able to produce the maximum number of output voltage levels with certain number of switches. In this algorithm, the number of voltage levels is more than all of the proposed algorithms in this paper remarkably, including the first and second cascade structures. The main purpose of this algorithm is to improve the quality of the output voltage waveform by using less number of switches. Value of DC voltage sources which used in the second cascade proposed structure is based on (36). The important equations of this algorithm are obtained in following and output voltage of each block is shown in table VI.

$$3V_{dc,3j} = 4V_{dc,(3j-1)} = 12V_{dc,(3j-2)} = 12(15^{j-1})V_{dc} \quad j=1,2,\dots, \quad (36)$$

$$N_{level} = 15^n \quad (37)$$

$$N_{variety} = 3n \quad (38)$$

$$V_{o,max} = \sum_{j=1}^n V_{dc,j}$$

$$= 3V_{dc} + 4V_{dc} + 45V_{dc} + 60V_{dc} + \dots + 3(15^{n-1})V_{dc} + 4(15^{n-1})V_{dc}$$

$$= \left(\frac{15^n - 1}{2}\right)V_{dc} \quad (39)$$

$$V_{block,Sn} = \begin{cases} 15^{n-1}V_{dc} & S_{1,n}, S'_{1,n} \\ 4(15^{n-1})V_{dc} & S_{2,n}, S'_{2,n} \\ 2(15^{n-1})V_{dc} & T_{1,n}, T'_{1,n} \\ 7(15^{n-1})V_{dc} & T_{2,n}, T'_{2,n} \end{cases} \quad (40)$$

$$\begin{aligned}
 V_{block} &= 2 \sum_{j=1}^n (V_{block,S1,j} + V_{block,S2,j} + V_{block,T1,j} + V_{block,T2,j}) \\
 &= 2(15^n - 1)V_{dc}
 \end{aligned} \quad (41)$$

In following IGBTs number, the number of DC voltage sources and variety of them for the first and second proposed structures are plotted versus number of output voltage levels in Fig. 3 and Fig. 4 respectively to have a comparison between proposed algorithms.

As can be seen in Fig. 3(a),  $A_4$  has the lowest IGBTs number among the proposed algorithms, so number of switches, diodes and drivers is lower than other algorithms, therefore number of power electronic components in  $A_4$  is less than others in first structure. The number of input DC voltage sources is compared in Fig. 3(b). As can be seen, number of DC voltage sources in  $A_4$  is less than other proposed algorithms too. Fig. 3(c) shows that the first algorithm has the lowest variety of DC voltage sources which has been proposed as one of the first algorithm benefits. According to materials which are mentioned above, the first ( $A_1$ ) and fourth ( $A_4$ ) algorithms of first cascade proposed structure is better than other mentioned algorithms. So in order to compare the first proposed structure with the conventional structures, these two algorithms are used.

From the Fig. 4(a), it is clear that required IGBTs number based on  $B_4$  is less than other algorithms for the second proposed structure. Therefore this algorithm has the least number of switches, diodes and drivers. In Fig. 4(b), the number of isolated DC voltage sources has been compared and it is clear that  $B_4$  in this term is better than other algorithms and consist of less number of sources for the same number of output voltage levels. As figure Fig. 4(c) shows, the third algorithm has the minimum variation of DC voltage sources for the low output voltage levels whereas the number of produced output voltage levels is less than fourth algorithm. According to the above comparison, the third ( $B_3$ ) and fourth ( $B_4$ ) algorithms of second cascade proposed structure are better than others. So in order to compare the second proposed structure with the traditional structures, these two algorithms are used.

### 3. Comparison Study

In this section, a comparison is done between proposed and conventional inverters to show advantages of proposed multilevel inverters. Topologies that are presented in [2-3], [9], [12] and CHB which are shown in Fig 5, have been selected to participate in this comparison. Each of the switches

in multilevel inverters, according to kind of them (unidirectional or bidirectional), consist of one or two IGBTs with one or two reverse diodes, and each of these switches needs to have a driver, thus reduction in the number of switches causes reduction in the size, weight and price of inverters. The number of switches in current-flow path to produce different voltage levels is another important factor which directly correlated with the conduction losses. In all the structures which are discussed in this section, current of switches is equal to the output load current, therefore, the structure that has less number of switches in current-flow path, has lower conduction losses. Another important factor to comparison of multilevel inverters is total blocked voltage by switches or normalized blocked voltage. It is clear that the lower blocked voltage of switches leads to reduce size and price of them. The number and variety of input DC voltage sources are important factors to compare multilevel inverters; a structure has better conditions, if the value of these parameters for a certain number of output voltage levels is reduced. In Fig 6, a comparison between the first and second cascade proposed structures and conventional structures is done in terms of number of IGBTs, diodes, DC voltage sources and component in current-flow path. Also in Fig 7 total blocked voltage, normalized blocked voltage and variety of DC voltage sources are plotted. {R1-2} To have a fair comparison between the structures which discussed in this article, DC voltage source selection in conventional structures is determined based on asymmetric algorithm that can generate the greatest number of output voltage levels.

It is obvious in Fig. 6(d), which structure [2] has the minimum number of components in current-flow path in comparison with other structures, but other parameters of this inverter don't have good features. Modularity and easy troubleshooting are the advantages of inverter [3], but blocked voltage and also variety of DC voltage sources in this structure is higher than other inverters.

CHB not only is modular also has advantages such as lower blocked voltage and no need to high number of DC voltage sources, but the number of power electronic switches and thus the number of drivers in this structure are more than others. Structure [9] is one of the newest structures, which has been proposed for cascade multilevel inverter. Required IGBTs number in this structure in comparison with conventional structures is significantly reduced, so that, among the proposed algorithms of first and second cascade structures, only  $B_4$  algorithm has less number of IGBTs compared to this inverter. In each block of [9], because of the position of input sources, two bidirectional switches are required, which leads to

increasing the number of IGBTs. In this inverter, instead of using two IGBTs, one IGBT and four power diodes are replaced which as can be seen in Fig. 6(b) and Fig. 6(d), lead to increasing number of diodes and components in current-flow path. Also high total blocked voltage of this structure is another disadvantage. Inverter [12] has the lower blocked voltage than other structures but the main disadvantage of this inverter is the high number of input voltage sources. According to comparisons in Fig. 6, it is obvious that algorithm  $B_4$  has the minimum number of IGBTs, diodes and also components in current-flow path is less than all proposed structures except structure [2].

The main disadvantage of this algorithm is high variety of input DC voltage sources which shown in Fig. 7(c). The algorithm  $A_1$  has the minimum variety of DC voltage sources but it should be noted that the number of output voltage levels for the same number of IGBTs is much less than algorithm  $B_4$ . Algorithms  $A_4$  and  $B_3$  have some intermediate features in comparison with Algorithms  $A_1$  and  $B_4$ .

In these algorithms, the required number of IGBTs is a little more than algorithm  $B_4$  but much less than the algorithm  $A_1$ . However, the value and variety of DC voltage sources is between them and algorithms  $A_4$  and  $B_3$  has the lowest variety of DC voltage sources regardless of algorithm  $A_1$ .

#### 4. Simulation Results

Although there are several modulation methods for multilevel inverters [23-24], in this paper, the fundamental frequency switching method has been used. It is important to note that the calculation of the optimal switching angles for selective harmonics elimination or minimization of total harmonic distortion (THD) is not the objective of this study. As mentioned in [1], relation between THD and number of output voltage levels can be obtained according to Fig. 9 in base frequency, thus THD of output voltage waveform can be decreased by increasing the number of output voltage levels regardless of modulation techniques.

In this section the output voltages and current of the algorithms  $A_4$  and  $B_4$  for the first and second proposed Submultilevel inverters are shown in Fig. 9. Also, to show the performance of the cascaded proposed structures, the first cascaded structure with two stages is used and the magnitude of the DC voltage sources is selected according to (17). The PSCAD/EMTDC software has been used for simulations.

##### 1. $A_4$ simulation

Since the number of output voltage levels is high in this algorithm, the first basic proposed

structure has been used. The magnitude of the DC voltage sources is considered according to (20) and  $V_{dc} = 25V$  is assumed. The output voltage and current waveforms based on this algorithm for the first proposed inverter are shown in Fig. 9(a). As can be seen from Fig. 9(a), the number of output voltage levels of the first proposed Submultilevel inverter in this algorithm is equal to 13 levels, which confirms accuracy of (21).

Table.1.  
Switching states of the first and second proposed Submultilevel inverters

s	ON Switches				$v_o$ (Fig.1(a))	$v_o$ (Fig.1(b))
1	$S_1$	$T_1$	$T_2$	$S_2$	$V_{dc,1} + V_{dc,2}$	$-V_{dc,1} + V_{dc,2}$
2	$S_1'$	$T_1'$	$T_2'$	$S_2'$	$-V_{dc,1} - V_{dc,2}$	$V_{dc,1} - V_{dc,2}$
3	$S_1$	$T_1$	$T_2$	$S_2'$	$V_{dc,1} + V_{dc,2} + V_{dc,3}$	$-V_{dc,1} + V_{dc,2} + V_{dc,3}$
4	$S_1'$	$T_1'$	$T_2'$	$S_2$	$-V_{dc,1} - V_{dc,2} - V_{dc,3}$	$V_{dc,1} - V_{dc,2} - V_{dc,3}$
5	$S_1$	$T_1$	$T_2'$	$S_2$	$V_{dc,1} - V_{dc,3}$	$-V_{dc,1} - V_{dc,3}$
6	$S_1'$	$T_1'$	$T_2$	$S_2'$	$-V_{dc,1} + V_{dc,3}$	$V_{dc,1} + V_{dc,3}$
7	$S_1$	$T_1$	$T_2'$	$S_2'$	$V_{dc,1}$	$-V_{dc,1}$
8	$S_1'$	$T_1'$	$T_2$	$S_2$	$-V_{dc,1}$	$V_{dc,1}$
9	$S_1$	$T_1'$	$T_2$	$S_2$	0	0
10	$S_1'$	$T_1$	$T_2'$	$S_2'$	0	0
11	$S_1$	$T_1'$	$T_2$	$S_2'$	$V_{dc,3}$	$V_{dc,3}$
12	$S_1'$	$T_1$	$T_2'$	$S_2$	$-V_{dc,3}$	$-V_{dc,3}$
13	$S_1$	$T_1'$	$T_2'$	$S_2$	$-V_{dc,2} - V_{dc,3}$	$-V_{dc,2} - V_{dc,3}$
14	$S_1'$	$T_1$	$T_2$	$S_2'$	$V_{dc,2} + V_{dc,3}$	$V_{dc,2} + V_{dc,3}$
15	$S_1$	$T_1'$	$T_2'$	$S_2'$	$-V_{dc,2}$	$-V_{dc,2}$
16	$S_1'$	$T_1$	$T_2$	$S_2$	$V_{dc,2}$	$V_{dc,2}$

Table.1.  
Maximum blocked voltage of first and second proposed Submultilevel inverters switches

Switches	$S_1 / S_1'$	$S_2 / S_2'$	$T_1 / T_1'$	$T_2 / T_2'$
First Structure	$V_{dc,1}$	$V_{dc,3}$	$V_{dc,1} + V_{dc,2}$	$V_{dc,2} + V_{dc,3}$
Second Structure	$V_{dc,1}$	$V_{dc,3}$	$V_{dc,2} - V_{dc,1}$	$V_{dc,2} + V_{dc,3}$

##### 2. $B_4$ simulation

In this simulation, the second cascaded proposed structure with one stage is used. The amplitude of the DC voltage sources is considered according to (36) in this algorithm. As can be seen from Fig. 9(b), the number of output voltage levels of the second proposed Submultilevel inverter is equal to 15 levels, which confirms validity of (37). It should be noted that the value of  $V_{dc}$  in this test is similar to previous simulation.

Table.2.  
Output voltage of submultilevel inverters based on A<sub>1</sub>

s	Output Voltage of Sub Multilevel Inverters				v <sub>o</sub>
	1	2	...	n	
1	3V <sub>dc</sub>	2V <sub>dc</sub>	...	3(7 <sup>n-1</sup> )V <sub>dc</sub>	(7 <sup>n</sup> -1)V <sub>dc</sub> / 2
2	2V <sub>dc</sub>	2V <sub>dc</sub>	...	3(7 <sup>n-1</sup> )V <sub>dc</sub>	(7 <sup>n</sup> -3)V <sub>dc</sub> / 2
⋮	...	...	...	...	...
(7 <sup>n</sup> +1)/2	0	0	...	0	0
⋮	...	...	...	...	...
7 <sup>n</sup> -1	-2V <sub>dc</sub>	-2V <sub>dc</sub>	...	-3(7 <sup>n-1</sup> )V <sub>dc</sub>	-(7 <sup>n</sup> -3)V <sub>dc</sub> / 2
7 <sup>n</sup>	-3V <sub>dc</sub>	-2V <sub>dc</sub>	...	-3(7 <sup>n-1</sup> )V <sub>dc</sub>	-(7 <sup>n</sup> -1)V <sub>dc</sub> / 2

Table.3.  
Output voltage of submultilevel inverters based on A<sub>2</sub>, A<sub>3</sub>, B<sub>1</sub>

S	Output Voltage of Sub Multilevel Inverters				v <sub>o</sub>
	1	2	...	n	
1	6V <sub>dc</sub>	6V <sub>dc</sub>	...	6V <sub>dc</sub>	6nV <sub>dc</sub>
2	6V <sub>dc</sub>	6V <sub>dc</sub>	...	5V <sub>dc</sub>	(6n-1)V <sub>dc</sub>
⋮	...	...	...	...	...
6n+1	0	0	...	0	0
⋮	...	...	...	...	...
12n	-6V <sub>dc</sub>	-6V <sub>dc</sub>	...	-5V <sub>dc</sub>	-(6n-1)V <sub>dc</sub>
12n+1	-6V <sub>dc</sub>	-6V <sub>dc</sub>	...	-6V <sub>dc</sub>	-6nV <sub>dc</sub>

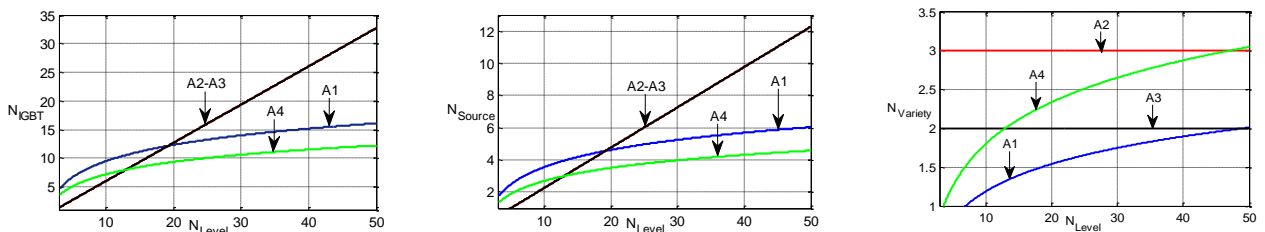


Fig. 3. Variations of a) IGBTs number b) DC voltage sources number and c) the variety of DC voltage sources versus number of output voltage levels in the first proposed structure according to various algorithms

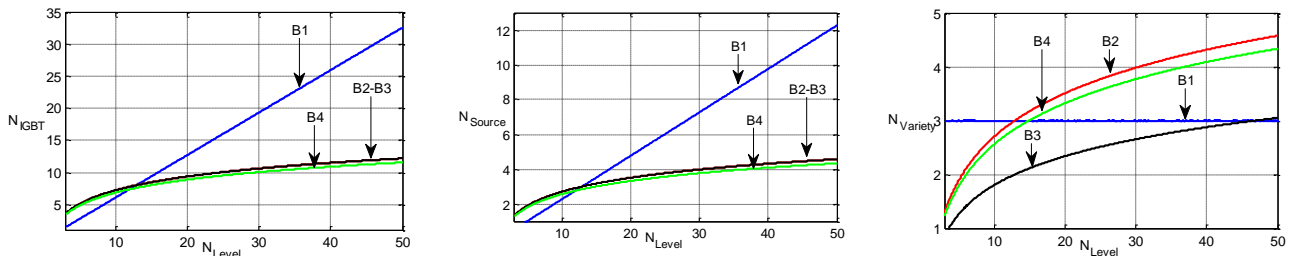


Fig. 4. Variations of a) IGBTs number b) DC voltage sources number and c) the variety of DC voltage sources versus number of output voltage levels in the second proposed structure according to various algorithms



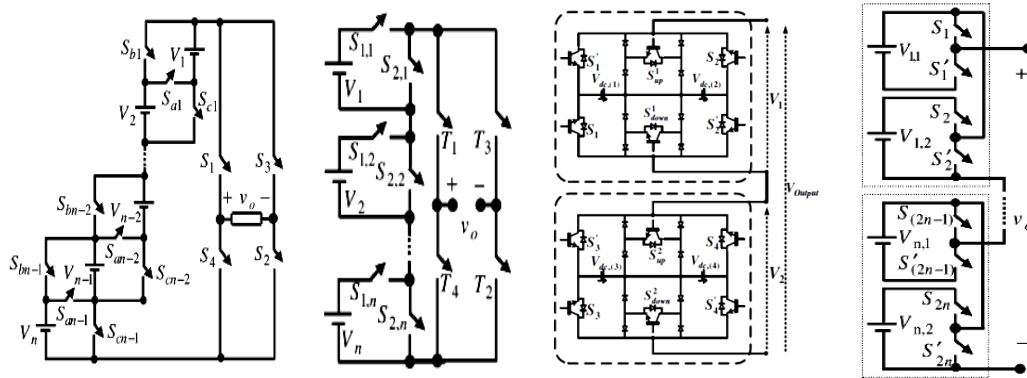


Fig. 5. Conventional multilevel inverters a) [2], b) [3], c) [9] and d) [12]

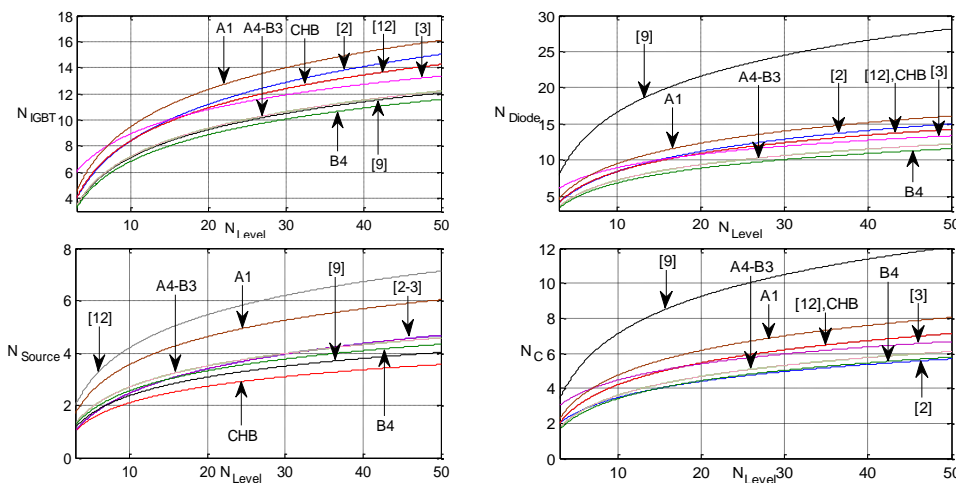


Fig. 6. Comparison between proposed cascade inverters with conventional inverters in terms of number of a) IGBTs, b) diodes, c) DC voltage sources and d) current path component

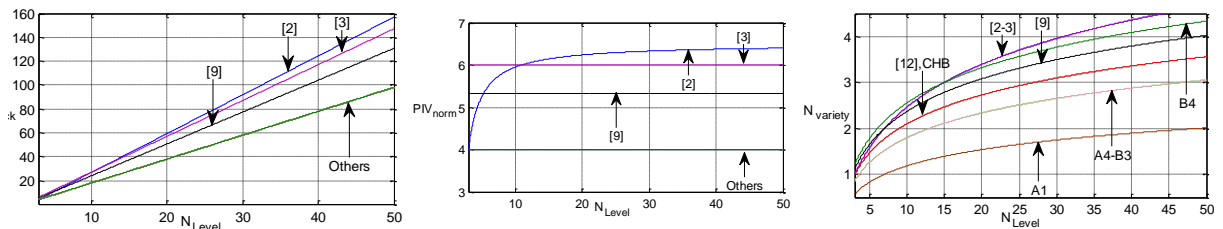


Fig. 7. Comparison between proposed inverters with conventional inverters in terms of a) total blocked voltage, b) normalized blocked voltage, and c) variety of DC voltage sources

Table.4.  
Output voltage of submultilevel inverters based on  $A_3, B_2, B_3$

State Number	Output Voltage of Sub Multilevel Inverters						$v_o$
	1	2	3	...	n-1	n	
1	$6V_{dc}$	$78V_{dc}$	$1014V_{dc}$	...	$6(13^{n-2})V_{dc}$	$6(13^{n-1})V_{dc}$	$(13^n - 1)V_{dc} / 2$
2	$5V_{dc}$	$78V_{dc}$	$1014V_{dc}$	...	$6(13^{n-2})V_{dc}$	$6(13^{n-1})V_{dc}$	$(13^n - 3)V_{dc} / 2$
...	...	...	...	...	...	...	...
$\frac{13^n + 1}{2}$	0	0	0	...	0	0	0
...	...	...	...	...	...	...	...
$13^n - 1$	$-5V_{dc}$	$-21V_{dc}$	$-1014V_{dc}$	...	$-6(13^{n-2})V_{dc}$	$-6(13^{n-1})V_{dc}$	$-(13^n - 3)V_{dc} / 2$
$13^n$	$-6V_{dc}$	$-21V_{dc}$	$-1014V_{dc}$	...	$-6(13^{n-2})V_{dc}$	$-6(13^{n-1})V_{dc}$	$-(13^n - 1)V_{dc} / 2$

Table.5.  
Output voltage of submultilevel inverters based on B<sub>4</sub>

State Number	Output Voltage of Sub Multilevel Inverters						$v_o$
	1	2	3	...	n-1	n	
1	$7V_{dc}$	$105V_{dc}$	$1575V_{dc}$	...	$7(15^{n-2})V_{dc}$	$7(15^{n-1})V_{dc}$	$(\frac{15^n - 1}{2})V_{dc}$
2	$6V_{dc}$	$105V_{dc}$	$1575V_{dc}$	...	$7(15^{n-2})V_{dc}$	$7(15^{n-1})V_{dc}$	$(\frac{15^n - 3}{2})V_{dc}$
⋮	...	...	...	...	...	...	...
$\frac{15^n + 1}{2}$	0	0	0	...	0	0	0
⋮	...	...	...	...	...	...	...
$15^n - 1$	$-6V_{dc}$	$-105V_{dc}$	$-1575V_{dc}$	...	$-7(15^{n-2})V_{dc}$	$-7(15^{n-1})V_{dc}$	$-(\frac{15^n - 3}{2})V_{dc}$
$15^n$	$-7V_{dc}$	$-105V_{dc}$	$-1575V_{dc}$	...	$-7(15^{n-2})V_{dc}$	$-7(15^{n-1})V_{dc}$	$-(\frac{15^n - 1}{2})V_{dc}$

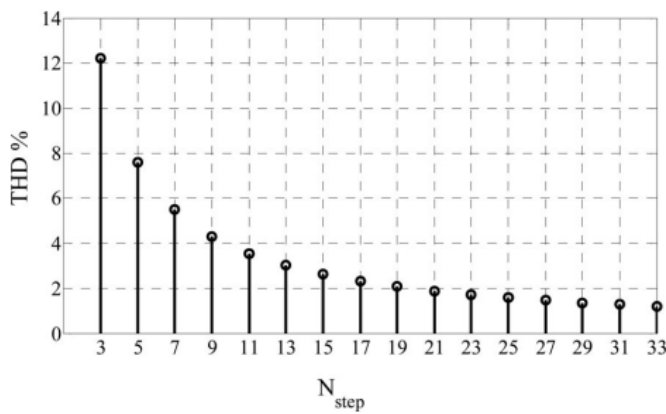


Fig. 8. THD of the output voltage waveform versus number of output voltage levels in base frequency

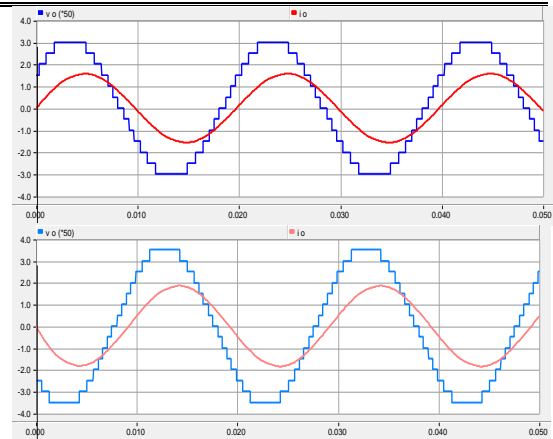


Fig. 9. Simulation of output voltage and current waveforms for a) the first proposed Submultilevel inverter and b) the second proposed Submultilevel inverter

## 5. Conclusion

In this paper, two new cascaded structures which are made of series Submultilevel inverter were proposed and four algorithms were proposed to determine the value of the DC voltage sources. By comparing all these algorithms, it was determined that the algorithms  $A_1$ ,  $A_4$ ,  $B_3$ , and  $B_4$  have better operation than the others. The selected algorithms of the proposed structures were compared with conventional structures in terms of the number of switches, the number of IGBTs, the number of diodes, the number of driver circuits, the blocked voltage of switches, the normalized blocked voltage, the number of current flow path components, the number of input voltage sources and variety of them. It showed that the proposed inverters consist less number of power electronic devices than the others. Therefore, the weight and size of the proposed inverters are reduced and they can be used for high power applications. Also due to the less number of components in current-flow path, proposed inverters have less conduction losses in comparison with the conventional structures. Finally, the simulation results were presented to confirm the operation accuracy of the proposed inverters.

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